What is Claimed is:

1. A method of fabricating a semiconductor integrated circuit device, comprising the steps of:

(a) forming two gate electrodes to be N- and P-type gate electrodes respectively over first and second regions of a silicon surface, each of said two gate electrodes having a silicon film to be a polysilicon conductive film;

(b) forming N-type source and drain regions in the first region, said N-type source and drain regions constituting a first insulated gate field effect transistor together with the N-type gate electrode;

(c) forming P-type source and drain regions in the second region, said P-type source and drain regions constituting a second insulated gate field effect transistor together with the P-type gate electrode doped with boron;

(d) depositing a Co film on the silicon surface over said N-type and P-type source regions and drain regions, and upper surfaces of said N- and P-type gate electrodes respectively isolated from said N-type and P-type source regions and drain regions with insulating side walls, by sputtering, from a Co sputtering target which, apart from carbon and oxygen impurities, is at least 99.99 wt.% pure, and wherein a sum of Fe and Ni in the Co sputtering target is not greater than 50 ppm by weight, wherein the sputtering is performed in such a manner that the composition of the deposited Co film is substantially the same as that of the Co sputtering target;

(e) performing first rapid thermal annealing at a first temperature to the silicon surface covered with the Co film so as to form Co monosilicide films on

the silicon surface and the upper surfaces, leaving a remaining Co film not formed into Co monosilicide, wherein the first temperature is a temperature that creep-up across the insulating side walls substantially does not take place;

(f) removing the remaining Co film, remaining over the first major surface, by wet etching; and

(g) after step (f), performing second rapid thermal annealing at a second temperature higher than the first temperature so as to form Co disilicide films on the silicon surface and the upper surfaces.

2. A method of fabricating a semiconductor integrated circuit device according to claim 1, wherein the first temperature is not higher than 525 degrees centigrade.

3. A method of fabricating a semiconductor integrated circuit device according to claim 2, wherein the second temperature is from 650 to 800 degrees centigrade.

4. A method of fabricating a semiconductor integrated circuit device according to claim 3, wherein the first temperature is not lower than 475 degrees centigrade.

5. A method of fabricating a semiconductor integrated circuit device according to claim 4, wherein the Co sputtering target includes a sum of Fe and

Ni which is not greater than 10 ppm by weight.

6. A method of fabricating a semiconductor integrated circuit device according to claim 5, wherein said Co sputtering target, apart from carbon and oxygen impurities, is 99.999 wt.% pure.

7. A method of fabricating a semiconductor integrated circuit device according to claim 1, wherein the Co sputtering target includes a sum of Fe and Ni which is not greater than 10 ppm by weight.

8. A method of fabricating a semiconductor integrated circuit device according to claim 1, wherein said Co sputtering target, apart from carbon and oxygen impurities, is 99.999 wt.% pure.